L73 ANSWER 18 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:490453 HCAPLUS
DN 129:183027
TI Stacked **floating gate** memory device
IN Clemens, James Theodore; Lee, Woo Hyong; Manchanda, Lalita
PA Lucent Technologies Inc., USA
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10189921	A2	19980721	JP 1997-277485	19971009
PRAI	US 1996-27612P	P	19961010		
	US 1996-871024	A	19961010		

AB The invention relates to a stacked **floating gate** memory device, i.e., **flash** memory, e.g., EPROM, wherein the IPD (inter-poly **dielec.**) layer interposed between the floating and **control gates** enables a erasing voltage .gtoreq. 5 V.
IT **1314-36-9**, Yttria, uses **1314-61-0**, Tantalum pentoxide **1344-28-1**, Alumina, uses
RL: DEV (Device component use); USES (Uses)
(IPD for stacked **floating gate** memory device)
RN 1314-36-9 HCAPLUS
CN Yttrium oxide (Y2O3) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 1314-61-0 HCAPLUS
CN Tantalum oxide (Ta2O5) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 1344-28-1 HCAPLUS
CN Aluminum oxide (Al2O3) (8CI, 9CI) (CA INDEX NAME)

L73 ANSWER 21 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:662969 HCAPLUS
DN 117:262969
TI Diffusionless source/drain conductor electrically **erasable**, electrically programmable read-only memory cells and arrays, and their use
IN Gill, Manzur
PA Texas Instruments Inc., USA
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5150179	A	19920922	US 1990-548045	19900705
	US 5284785	A	19940208	US 1992-842933	19920227
PRAI	US 1990-548045		19900705		

AB The ROM cell is formed at a face of a semiconductor layer, and includes a thin **dielec.** layer overlying at least the channel region; source and drain conductors (preferably doped polysilicon) spaced to define the channel region, which form and control source and drain inversion regions in the semiconductor layer; a thin oxide **tunneling** window in the channel adjacent to the source inversion region; a floating **gate** overlying at least a portion of the channel to control its conductance and the thin oxide **tunneling** window for **Fowler-Nordheim tunneling**; and a **gate** conductor insulatively adjacent to the floating **gate**. The cell (or array) is programmed, read, and **erased** by applying appropriate voltages to the appropriate conductors to charge or discharge the floating **gate** by **Fowler-Nordheim tunneling**.
IT **7440-21-3**, Silicon, uses
RL: PRP (Properties)
(polycryst., source and drain conductors from doped, in diffusionless elec. **erasable**, elec. programmable ROM cells and arrays)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L74 ANSWER 3 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:865969 HCAPLUS
TI Method for operation of a **flash** memory using n+/p-well diode
IN Chi, Min-hwa
PA Worldwide Semiconductor Manufacturing Corporation, Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L029-78
ICS H01L033-00
NCL 257315000
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6160286	A	20001212	US 1999-422050	19991020

AB A **flash** memory cell formed in a semiconductor substrate is disclosed. The cell includes a deep n-well formed within the substrate. Next, a p-well is formed within the deep n-well and a n+ drain region is formed within the p-well. A **floating gate** is formed above the p-well being separated from the substrate by a thin oxide layer. The **floating gate** is formed adjacent to the n+ drain region. Finally, a **control gate** is formed above the **floating gate**, the **floating gate** and the **control gate** being separated by a **dielectric** layer. The new cell is read by measuring the GIDL current at n+/p-well junction, which is exponentially modulated by the **floating gate** potential (or its net charge). The new cell is programmed by substrate **hot electron injection** and is **erased** by **F-N tunneling** through the overlap area of **floating gate** and p-well.

RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
RE
(1) Bergemont; US 5847426 1998 HCAPLUS
(2) Chen; US 5814853 1998 HCAPLUS

L74 ANSWER 4 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:547161 HCAPLUS
DN 127:143798
TI Fabrication of nonvolatile **flash**-memory devices for writing/**erasing** by **F-N tunnel** current
IN Yamauchi, Yoshimitsu
PA Sharp Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L027-115
ICS H01L021-8247; H01L029-788; H01L029-792
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 09162374	A2	19970620	JP 1995-319174	19951207

AB The title memory devices have a memory cell matrix each comprising a **tunnel** oxide film, a floating agate, an insulator film, a **control gate**, and source/drain, wherein the **control gates** are connected in a x-direction and the source/drain in a y-direction connected via doped diffusion bit lines in the matrix. The fabrication involves forming dopant diffusion layers each extended to source/drain regions and a y-direction on a substrate, forming an oxide film in self-alignment to the doped diffusion layer, forming a **tunnel** oxide film each across the doped diffusion layers, forming a 1st **gate** layer on the **tunnel** oxide film and partly over the **tunnel** oxide film, depositing a 2nd **gate** layer via an insulator film over the entire surface, and subsequently etching the 2nd **gate** layer, the **floating gate**, and the 1st **gate** layer successively over a patterned mask to form the **control gate** and the **floating gate**. The process by the self alignment provides the oxide films over the bit lines in fine and precision formation.
ST bit line oxide nonvolatile memory device; **tunnel** current nonvolatile **flash** memory device
IT **Tunneling** current
(F-N; fabrication of nonvolatile **flash**-memory devices for writing/**erasing** by **F-N tunnel** current)
IT Memory devices
(fabrication of nonvolatile **flash**-memory devices for writing/**erasing** by **F-N tunnel** current)
IT **Dielectric** films
(oxide, nitride; fabrication of nonvolatile **flash**-memory devices for writing/**erasing** by **F-N tunnel** current)

L74 ANSWER 5 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:418184 HCAPLUS
DN 125:102859
TI Method of making an EEPROM cell with separate **erasing** and programming regions
IN Gill, Manzur; Mcelroy, David J.; Lin, Sung Wei; Lee, Inn K.
PA Texas Instruments Incorporated, USA
SO U.S., 16 pp. Cont. of U.S. Ser. No. 82,659, abandoned.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-8247
NCL 437043000
CC 76-14 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5523249	A	19960604	US 1994-364529	19941223
PRAI	US 1990-560950		19900801		
	US 1991-723735		19910620		
	US 1992-908610		19920629		
	US 1993-82659		19930625		

AB An elec.-**erasable**, elec.-programmable, read-only-memory cell array is formed in pairs at a face of a semiconductor substrate (22). Each memory cell includes a source region (11) and a drain region (12), with a corresponding channel region between. A **Fowler-Nordheim tunnel**-window (13a) is located over the source line (17) connected to source (11). A floating **gate** (13) includes a **tunnel**-window section. A control **gate** (14) is disposed over the floating **gate** (13), insulated by an intervening inter-level **dielec.** (27). The floating **gate** (13) and the control **gate** (14) include a channel section (Ch). The channel section (Ch) was used as a self-alignment implant mask for the source (11) and drain (12) regions, such that the channel-junction edges are aligned with the corresponding edges of the channel section (Ch). The memory cell is programmed by hot-carrier injection from the channel to the floating **gate** (13), and **erased** by **Fowler-Nordheim tunneling** from the floating **gate** (13) through the **tunnel** window (13a) to the source-line (17). The program and **erase** regions of the cells are phys. sep. from each other, and the characteristics, including the oxides, of each of those regions may be made optimum independently from each other.

ST EEPROM memory cell **Fowler Nordheim tunnel**
IT Memory devices
(read-only, making EEPROM cells with sep. **erasing** and programming regions)

L74 ANSWER 6 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:497713 HCAPLUS
DN 121:97713
TI Nonvolatile semiconductor memory cell
IN Chen, Ling; Lin, Tien Ler; Wu, Albert
PA Integrated Silicon Solution, Inc., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L029-68
ICS H01L029-78; H01L029-34
NCL 257321000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5317179	A	19940531	US 1991-764019	19910923
	US 5453388	A	19950926	US 1993-132941	19931007
PRAI	US 1991-764019		19910923		

AB Described in a **flash** EEPROM cell needing only a 5 V external source using an on-chip voltage multiplier circuit to provide high voltages necessary to effect **Fowler-Nordheim tunneling** during both the program and **erase** modes. Properties of **dielec.** layers between a **floating gate** and a **control gate** and between the **floating gate** and a drain region differ to facilitate programming and **erasing** of the **floating gate**. A method for producing the cell involves forming the insulative layer between a **floating gate** and a **control gate** to have a capacitance lower than the capacitance of the insulating layer between the **floating gate** and a drain region.

ST nonvolatile semiconductor memory cell; **flash** EEPROM cell
IT Memory devices
(read-only, elec. **erasable** programmable, **flash**, prodn. of)

L73 ANSWER 5 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:687502 HCAPLUS
DN 135:234901
TI Electrically **erasable** and programmable read only memory device with enhanced source side **Fowler-Nordheim tunneling effect** and manufacturing therefor
IN Peng, Nai-Chen
PA United Microelectronics Corp., Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6291854	B1	20010918	US 1999-474997	19991230

AB A fabrication method for an elec. **erasable** programmable read only memory is described in which the memory cell has a sharp-cornered polysilicon pillar in junction with the source region to enhance the source side **Fowler-Nordheim tunneling effect**. The fabrication method sequentially forms an oxide layer and a Si nitride on a Si substrate, and then patterns the oxide layer and the Si nitride layer to form a plurality of trenches. A 1st doped polysilicon layer is then formed on the substrate and fills the trenches. A wet oxidn. is then conducted to grow an oxide layer on the 1st doped polysilicon layer, from which a sharp-cornered doped polysilicon layer results. A 1st **dielec.** layer is further formed on the substrate and the doped polysilicon layer, followed by forming a floating **gate** on the 1st **dielec.** layer. After this, a 2nd **dielec.** layer is formed on the substrate, covering the floating **gate**, and a control **gate** is formed on the 2nd **dielec.** layer.

IT **7440-21-3**, Silicon, processes **7631-86-9**, Silica, processes **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(elec. **erasable** and programmable read only memory device with enhanced source side **Fowler-Nordheim tunneling effect** and manufg. therefor)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L73 ANSWER 23 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1987:167072 HCAPLUS
DN 106:167072
TI A true single-transistor oxide-nitride-oxide EEPROM device
AU Chan, T. Y.; Young, K. K.; Hu, Chenming
CS Dep. Electr. Eng. Comput. Sci., Univ. California, Berkeley, CA, 94720, USA
SO IEEE Electron Device Lett. (1987), EDL-8(3), 93-5
CODEN: EDLEDZ; ISSN: 0193-8576
DT Journal
LA English
AB A novel single-transistor EEPROM (elec. EPROM) device using single-polysilicon technol. is described. This memory is programmed by **channel hot-electron injection** and the charges are stored in the oxide-nitride-oxide (ONO) **gate dielec.** **Erasing** is accomplished in ms by applying a pos. voltage to the drain plus an optional neg. voltage to the **gate** causing electron **tunneling** and/or hot-hole injection due to the deep-depletion-mode drain breakdown. Since the injection and storage of electrons and holes are confined to a short region near the drain, the part of the channel near the source maintains the original pos. threshold voltage even after repeated **erase** operations. Therefore a select transistor, sep. or integral, is not needed. Because oxide layers with a thickness > 60 .ANG. are used, this device has much better data retention characteristics than conventional MNOS memory cells. This device was successfully tested for **WRITE /ERASE** endurance to 10,000 cycles.
IT **7440-21-3**, Silicon, uses and miscellaneous **11126-22-0**, Silicon oxide **12033-89-5**, Silicon nitride, uses and miscellaneous
RL: USES (Uses)
(memory device contg., single-transistor elec. **erasable** programmable read-only)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

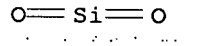
Si

RN 11126-22-0 HCAPLUS
CN Silicon oxide (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
O	x	17778-80-2
Si	x	7440-21-3

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L73 ANSWER 8 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:401359 HCAPLUS
DN 135:130238
TI A novel P-channel **flash** electrically-**erasable** programmable read-only memory (EEPROM) cell with oxide-nitride-oxide (ONO) as split **gate** channel **dielectric**
AU Huang, Chih-Jen; Liu, Yun-Chang; Wang, Mu-Chun; Caywood, John; Hong, Shi-Fang; Wu, Auter; Hsia, Liang-Chu; Chang, Yi-Jao; Liu, Fu-Tai
CS Technology and Process Development Division, United Microelectronics Corp., Hsin-Chu, Taiwan
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (2001), 40(4B), 2943-2947
CODEN: JAPNDE; ISSN: 0021-4922
PB Japan Society of Applied Physics
DT Journal
LA English
AB A novel p-channel **flash** elec.-**erasable** programmable read-only memory (EEPROM) cell, which is programmed/**erased** via channel **Fowler-Nordheim** (FN) **tunneling**, is described. Channel FN **tunneling** is a high efficiency and low-power-consumption approach to **flash** cell operation. High endurance up to 1 M cycles was demonstrated with small window closure. The new **flash** cell exhibits good reliability which is quite insensitive to disturb or over program. In order to simplify the process, the interpoly **dielec.** and select **gate dielecs** . are fabricated using the same oxide-nitride-oxide (ONO) stack during formation of this cell. Hence, this cell shows good potential for achieving simple processing, low power consumption and negligible disturbance during operation.
IT **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(ONO structure; a novel P-channel **flash** elec.-**erasable** programmable read-only memory (EEPROM) cell with oxide-nitride-oxide (ONO) as split **gate** channel **dielec.**)
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)



RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L73 ANSWER 9 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:247870 HCAPLUS
DN 134:319240
TI Conduction properties of electrically **erasable** read only memory **tunnel** oxides under dynamic stress
AU Plossu, C.; Croci, S.; Monti, N.; Bouchakour, R.; Laffont, R.; Boivin, Ph.; Mirabel, J. M.
CS Laboratoire de Physique de la Matiere (LPM), UMR CNRS 5511, Institut National des Sciences Appliquees de Lyon, Villeurbanne, F-69621, Fr.
SO Journal of Non-Crystalline Solids (2001), 280(1-3), 103-109
CODEN: JNCSBJ; ISSN: 0022-3093
PB Elsevier Science B.V.
DT Journal
LA English
AB The **write** and **erase** programmable operations in elec. **erasable** read only memories (EEPROM) which are based on **Fowler-Nordheim tunneling** injection through a thin **tunnel** oxide window were reproduced on specific large area double polycryst. (poly) test capacitors. These structures integrate the different stacked layers (upper control **gate** polysilicon layer; interpoly **dielec.** layer; floating **gate** polysilicon layer; **tunnel** oxide; N+ substrate) of the active area of a memory cell state transistor. Stress pulses similar to those used in the programming memory cells were applied to the upper polysilicon layer. The variations of the **tunnel** oxide elec. conduction properties after numerous **write-erase** cycles were studied by measuring the current as a function of voltage characteristics of the structure. The **Fowler-Nordheim** consts. were obtained as a function of the no. of stress cycles. A model based on a simple equiv. elec. circuit was then implemented to simulate the resulting variations of the floating polysilicon **gate** charge and of the threshold voltage of the structure in both **write** and **erase** modes. These variations were compared to those directly measured on a memory cell. The closure of the programmable window in memory devices can be unambiguously attributed to a decrease of the **tunnel** oxide cond.
IT **7440-21-3**, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(conduction properties of elec. **erasable** read only memory **tunnel** oxides under dynamic stress)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IT **7631-86-9**, Silica, properties **11105-01-4**, Silicon nitride oxide
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(conduction properties of elec. **erasable** read only memory **tunnel** oxides under dynamic stress)
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

RN 11105-01-4 HCAPLUS
CN Silicon nitride oxide (9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L73 ANSWER 10 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:237387 HCAPLUS
DN 134:373653
TI Photoemission study of energy band alignment and gap state density distribution for high-k **gate dielectrics**
AU Miyazaki, Seiichi; Hirose, Masataka
CS Department of Electrical Engineering, Hiroshima University, Higashi-Hiroshima, 739-8527, Japan
SO AIP Conference Proceedings (2001), 550(Characterization and Metrology for ULSI Technology), 89-96
CODEN: APCPCS; ISSN: 0094-243X
PB American Institute of Physics
DT Journal
LA English
AB The energy band gaps of thin high-**dielec.-const.** (high-k) insulators such as Ta2O5, Si3N4 and Al2O3 were detd. by measuring the energy loss spectra of O1s or N1s photoelectrons. From the anal. of the valence band spectra for thin high-k **dielecs.** prepd. on metals and Si(100), the energy band profiles for metal/high-k **dielec.**/Si(100) systems were detd. in consideration for the measured energy bandgaps and metal work functions. Intrinsic **tunneling** leakage currents for TiN/Ta2O5/SiO2/Si(100) and Al/Al2O3/Si(100) systems were calcd. by applying a transfer matrix method to their energy band profiles so detd. The results show that, for the TiN/Ta2O5/SiO2/Si(100) structure, the interfacial SiO2 layer is a crucial factor to suppress the electron **tunneling** rate, while for the Al/Al2O3/Si(100) structure the **tunneling** current is sufficiently low even in an SiO2-equivalent thickness of 1.2 nm compared with conventional n+-poly Si/SiO2/Si(100). Also total photoelectron yield spectroscopy is a useful and high-sensitive technique to evaluate the energy distribution of defect states in the high-k **dielecs.** and at the interfaces.
IT **7429-90-5**, Aluminum, uses **7440-21-3**, Silicon, uses **7440-25-7**, Tantalum, uses **25583-20-4**, Titanium nitride
RL: DEV (Device component use); USES (Uses)
(photoemission study of energy band alignment and gap state d. distribution for high-k **gate dielecs.**)
RN 7429-90-5 HCAPLUS
CN Aluminum (8CI, 9CI) (CA INDEX NAME)

Al

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L73 ANSWER 15 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:439371 HCAPLUS
DN 131:66552
TI Electronic components with doped metal oxide **dielectric** materials and a process for making MOS devices with doped metal oxide **dielectric** materials
IN Lee, Woo-hyeong; Manchanda, Lalita
PA Lucent Technologies Inc., USA
SO U.S., 6 pp., Cont.-in-part of U.S. Ser. No. 871,024.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5923056	A	19990713	US 1998-41434	19980312
	JP 11297867	A2	19991029	JP 1999-65742	19990312
PRAI	US 1996-27612P	P	19961010		
	US 1997-871024	A2	19970606		
	US 1998-41434	A	19980312		

AB A doped, metal oxide **dielec.** material and electronic components made with this material are disclosed. The metal oxide is a Group III or Group VB metal oxide (e.g. Al2O3, Y2O3, Ta2O5 or V2O5 and the metal dopant is a Group IV material (Zr, Si, Ti, and Hf)). The metal oxide contains .apprx.0.1 to .apprx.30 wt.% of the dopant. The doped, metal oxide **dielec.** of the present invention was used in a no. of different electronic components and devices. For example, the doped, metal oxide **dielec.** was used as the gate **dielec.** for MOS devices. The doped, metal oxide **dielec.** is also used as the inter-poly **dielec.** material for **flash memory** devices.

IT **1314-36-9**, Yttrium oxide (Y2O3), uses **1314-61-0**, Tantalum oxide (Ta2O5) **1314-62-1**, Vanadium oxide (V2O5), uses **1344-28-1**, Aluminum oxide (Al2O3), uses
RL: DEV (Device component use); USES (Uses)
(electronic components with doped metal oxide **dielec.** materials and process for making MOS devices with doped metal oxide **dielec.** materials)

RN 1314-36-9 HCAPLUS
CN Yttrium oxide (Y2O3) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***

RN 1314-61-0 HCAPLUS
CN Tantalum oxide (Ta2O5) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***

RN 1314-62-1 HCAPLUS
CN Vanadium oxide (V2O5) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***

RN 1344-28-1 HCAPLUS
CN Aluminum oxide (Al2O3) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***

IT **7440-21-3**, Silicon, uses **7440-32-6**, Titanium, uses **7440-58-6**, Hafnium, uses **7440-67-7**, Zirconium, uses
RL: MOA (Modifier or additive use); USES (Uses)
(electronic components with doped metal oxide **dielec.** materials and process for making MOS devices with doped metal oxide **dielec.** materials)

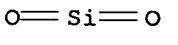
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

L73 ANSWER 19 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:331413 HCAPLUS
DN 129:22187
TI Method of making EEPROM cell having improved **control gate-floating gate** coupling ratio
IN Hsu, Louis Lu-chen; Ogura, Seiki; Peng, James
PA International Business Machines Corp., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5753525	A	19980519	US 1995-579025	19951219

AB A method of forming EEPROM cells is described. The method includes forming a **tunnel** oxide layer on a wafer and forming **floating gates** on the **tunnel** oxide layer with the **floating gate** having sidewalls. Isolation regions may be formed adjacent to the sidewalls. A conformal ONO layer of **dielec.** is formed on the **floating gate** and sidewalls, using CVD. Next, a selective etch material layer is deposited on the wafer over the conformal **dielec.** layer. A polish stop layer is deposited on the wafer over the selective etch material layer to define an upper polishing surface above the **floating gate.** The exposed polish stop layer and underlying selective etch material are removed by depositing an oxide layer on the polish stop layer and then polishing the deposited layer coplanar with the polish stop layer which is an upper polishing surface above the **floating gates.** Exposed portions of the polish stop layer are removed to expose the selective etch layer above the **floating gates** and above sidewall regions adjacent the sidewalls. Then, the exposed selective etch layer is removed, exposing the conformal **dielec.** layer. Finally, a **control gate** may be formed by depositing a **control gate** layer above the **floating gate** and within the sidewall region and patterning the **control gate** layer. The patterned **control gates** extend over the **floating gate** and along the **floating gate** sidewalls. The **control gate-floating gate** capacitor area includes the **floating gate** sidewalls.

IT **7631-86-9,** Silica, processes **12033-89-5,** Silicon nitride (Si3N4), processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method of making EEPROM cell having ONO **dielec.** layer contg.)
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)



RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
IT **7440-21-3,** Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical

process); PROC (Process); USES (Uses)
(method of making EEPROM cell with improved **control gate-floating gate** coupling ratio)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IT **1344-28-1**, Aluminum oxide, processes **10043-11-5**, Boron nitride, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(selective etch material; method of making EEPROM cell with improved **control gate-floating gate** coupling ratio)

L74 ANSWER 1 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:71758 HCAPLUS
DN 136:127648
TI **Erasure** process in **flash** memory cells having laminated **gates**
IN Lee, Hee Yeul
PA Hynix Semiconductor Co., Ltd., S. Korea
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC H01L021-8247; H01L027-115; H01L029-788; H01L029-792
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2002026158	A2	20020125	JP 2001-86865	20010326
PRAI KR 2000-36519	A	20000629		

AB The title cell comprises (1) a (**tunnel** oxide/**floating gate**/**dielec.**/**control gate**)-laminated **gate** formed on a well-contg. semiconductor substrate and (2) contact regions each formed across the laminated **gate**. The memory in the memory cells are (1) programmed by **injecting hot electron** into the **floating gate** and (2) **erased** by FN-**tunneling** between the **floating gate** and the semiconductor substrate. The **erasing** process involves (A) impressing a neg. bias voltage on the **control gate** and a pos. bias voltage on the well to give the contact regions floating and (B) impressing ground voltage on the well, the **control gate**, and the contact regions successively. The **erasing** process in the memory cells is enhanced by the parasitic capacitance provided between the contact regions and the well and consequently makes possible the **tunnel** oxide film and the **dielec.** film increased.

ST parasitic capacitance memory cell **erasing** enhancement contact region well

IT Memory effect
(**erasing** of, by FN **tunneling**; **erasure** process in **flash** memory cells having laminated **gates**)

IT Memory devices
(**flash**, **erasing** of; **erasure** process in **flash** memory cells having laminated **gates**)

IT Transistors
(laminated **gate**; **erasure** process in **flash** memory cells having laminated **gates**)

IT Electric potential
(neg./pos. bias voltage impression on memory cells; **erasure** process in **flash** memory cells having laminated **gates**)

Assignee

FILE 'INPADOC, WPIX, JAPIO, HCAPLUS, TULSA' ENTERED AT 16:19:47 ON 08 APR 2002

E TW2001-90110699/PRN,AP
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E TW01-90110699/AP
E TW2001-110699/AP
E TW2001-110699/PRN
E TW2001-90110699/PRN

L1	690	SEA ABB=ON PLU=ON MACRONIX?/CS,PA
L2	2	SEA ABB=ON PLU=ON L1 AND FLASH MEMORY STRUCTURE
		D ALL TOT
		D MAX 2
L3	65	SEA ABB=ON PLU=ON L1 AND FLASH MEMORY/TI
L4	14	SEA ABB=ON PLU=ON L3 AND PY>2000
L5	12	SEA ABB=ON PLU=ON L4 NOT L2
L6	8	SEA ABB=ON PLU=ON L5 AND (FLOATING GATE OR BAND GAP OR BAND GAP OR GAP)
L7	8	SEA ABB=ON PLU=ON L5 AND (FLOATING GATE OR BANDGAP OR GAP)
L8	8	SEA ABB=ON PLU=ON L7 NOT L2
		D ALL TOT

L2 ANSWER 2 OF 2 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2001-578154 [65] WPIX
DNN N2001-430070 DNC C2001-171742
TI Reducing source enhanced gate disturb in common source **flash memory structure** where ion implantation concentration used for forming source is lower than that for forming drain.
DC L03 U11
IN CHEN, B; HUANG, J; JANG, Y; TSAI, Y
PA (MACR-N) **MACRONIX INT CO LTD**
CYC 1
PI TW 430884 A 20010421 (200165)* H01L021-265
ADT TW 430884 A TW 1999-102386 19990219
PRAI TW 1999-102386 19990219
IC ICM H01L021-265
AB TW 430884 A UPAB: 20011108
NOVELTY - A method for reducing source enhanced gate disturb in common source flash memory is described. The ion implantation concentration used in the ion implantation step for forming the source of the flash memory is lower than that for forming the drain. Through such asymmetrical ion implantation, the probability of FN tunneling is reduced and furthermore the accumulated source voltage is also decreased, thereby reducing the threshold voltage disturb on the non-programmed memory cells.
Dwg.1/1
FS CPI EPI
FA AB; GI
MC CPI: L03-G04A; L04-C02B
EPI: U11-C02B2

L8 ANSWER 5 OF 8 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1998-018755 [02] WPIX
DNN N1998-014239
TI **Floating gate flash memory**
integrated circuit - supplying first and second erase voltage sequences to memory cells to control band-to-band tunnelling current encountered during erase process.
DC U12 U13 U14
IN CHEN, H S; CHUANG, W; HUNG, C H; LIU, Y; SHIAU, T; SHONE, F; WAN, R; CHEN, H; LIN, J; LIN, Y; TSAI, C; HUNG, C; WAN, R L
PA (MACR-N) **MACRONIX INT CO LTD**
CYC 26
PI WO 9744791 A1 19971127 (199802)* EN 37p G11C011-34
RW: AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP US
US 5699298 A 19971216 (199805) 17p G11C016-00
EP 840929 A1 19980513 (199823) EN G11C011-34
R: DE FR GB IT
US 5787039 A 19980728 (199837)# G11C016-06
EP 863514 A2 19980909 (199840)# EN G11C016-06
R: AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 11509955 W 19990831 (199946) 40p G11C016-02
JP 11273366 A 19991008 (199954)# 56p G11C016-02
EP 840929 B1 20011219 (200206) EN G11C011-34 <--
R: DE FR GB IT
DE 69618206 E 20020131 (200216) G11C011-34 <--
PRAI WO 1996-US7490 19960522; US 1997-812615 19970306; EP 1998-301649 19980305; JP 1998-93810 19980303
IC ICM G11C011-34; G11C016-00; G11C016-02; G11C016-06
ICS G11C007-00
AB WO 9744791 A UPAB: 20000105
The IC comprises an array **floating gate** memory cells that have a high threshold state in which cells are not conductive and a low threshold state in which cells are conductive, in response to a read potential applied to control gate terminals of the cells. The cells also include drain lines coupled to the drain terminals (13,14) of columns of cells in the array, several source lines coupled to source terminals of respective columns, and several word lines (WL0-WLn) coupled to the control gate terminals of respective cell rows.

A control circuit is coupled to the drain lines, source lines and word lines, for setting in parallel the cells that are in a high threshold state to a low threshold state, and includes circuits supplying a voltage sequence to lower the thresholds of cells by Fowler-Nordheim tunnelling. If any of the cells are not in the low threshold state after a number M of retries of the voltage sequence, the circuits supply a second voltage sequence to lower the thresholds of cells by Fowler-Nordheim tunnelling. If all the cells are not in the low threshold state, then the second voltage sequence is retried until all the cells are in the low threshold state, or until a maximum number of retries has been executed.

ADVANTAGE - Reduces peak current consumption during erase process while maintaining erasing speed.

Dwg.2/9
FS EPI
FA AB; GI
MC EPI: U12-D02A1; U12-Q; U13-C04B2; U14-A03B7; U14-A07B

L8 ANSWER 4 OF 8 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1998-193893 [17] WPIX
CR 1998-193929 [17]; 1999-571426 [48]
DNN N1998-153417
TI Non-volatile memory block pre-programming method for **flash memory** - sets word lines coupled to control gates of memory cells in block to pre-program word line potential and applies pre-program channel potential to channel well of cells.
DC U13 U14
IN CHENG, Y; HUNG, C H; LEE, I; SHIAU, T; SHONE, F; WAN, R
PA (MACR-N) **MACRONIX INT CO LTD**
CYC 19
PI WO 9810424 A1 19980312 (199817)* EN 41p G11C011-34
RW: AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: JP US
EP 925586 A1 19990630 (199930) EN G11C011-34
R: FR GB IT NL
JP 2001500658 W 20010116 (200107) 42p G11C016-02 <--
ADT WO 9810424 A1 WO 1997-US3861 19970310; EP 925586 A1 EP 1997-915919 19970310, WO 1997-US3861 19970310; JP 2001500658 W WO 1997-US3861 19970310, JP 1998-512612 19970310
FDT EP 925586 A1 Based on WO 9810424; JP 2001500658 W Based on WO 9810424
PRAI WO 1996-US14349 19960905
IC ICM G11C011-34; G11C016-02
ICS G11C007-00; G11C016-04
AB WO 9810424 A UPAB: 20010202
The method involves setting word lines (413), coupled to control gates of memory cells in a block (403), to a pre-program word line potential. A pre-program potential is applied to a channel well (402-1 - 402-4) of memory cells to induce transfer of electrons to set charge levels in the **floating gates** to establish a pre-programmed state for the cells in the block.

The pre-programming is then verified with the block including several rows and columns of cells in which rows of cells in the block are coupled with corresponding word lines, and columns of cells are coupled to corresponding bit lines (419). When setting the word lines to the pre-program word line potential the word lines corresponding to the rows are set to the pre-program word line potential.

ADVANTAGE - Fast pre-programming speed, and suitable for low supply voltages.

Dwg.4/7
FS EPI
FA AB; GI
MC EPI: U13-C04B2; U14-A03B7; U14-A07B

L8 ANSWER 3 OF 8 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1999-543142 [46] WPIX
DNN N1999-402854
TI **Floating gate** transistor **flash** **memory** with substrate band-to-band tunneling induced hot electron injection.
DC U12 U14
IN GUO, J; TSAI, W J
PA (MACR-N) **MACRONIX INT CO LTD**; (GUOJ-I) GUO J; (TSAI-I) TSAI W J
CYC 27
PI EP 948058 A1 19991006 (199946)* EN 30p H01L029-788
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 11297865 A 19991029 (200003)# 60p H01L021-8247
US 6009017 A 19991228 (200007) G11C016-04
US 2001002052 A1 20010531 (200131) G11C016-04 <--
ADT EP 948058 A1 EP 1998-302631 19980403; JP 11297865 A JP 1998-111290 19980318; US 6009017 A US 1998-41807 19980313; US 2001002052 A1 Div ex US 1998-41807 19980313, Div ex US 1999-473849 19991228, US 2001-753788 20010103
FDT US 2001002052 A1 Div ex US 6009017
PRAI US 1998-41807 19980313; JP 1998-111290 19980318; US 1999-473849 19991228; US 2001-753788 20010103
IC ICM G11C016-04; H01L021-8247; H01L029-788
ICS H01L027-115; H01L029-792
AB EP 948058 A UPAB: 19991110
NOVELTY - The method involves inducing a flow of electrons into a **floating gate** of a transistor by inducing a band-to-band tunneling current from the semiconductor body (12) to either the source (13) or the drain (14) near the channel. A positive bias voltage is applied to the control gate (17) to induce hot electron injection into the **floating gate** (15).
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also given for
(a) a **floating gate** memory device.
(b) a method for manufacturing a **floating gate** memory device.
USE - For programming a non-volatile memory e.g. flash memory.
ADVANTAGE - Increases the speed and efficiency of programming a **floating gate** memory array. Operates at low supply voltages.
DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section of a triple well flash memory cell.
semiconductor body 12
source 13
drain 14
floating gate 15
control gate 17
Dwg.1/13
FS EPI
FA AB; GI
MC EPI: U12-D02A1; U14-A03B7; U14-A07B

L8 ANSWER 2 OF 8 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 2001-519771 [57] WPIX
DNN N2001-384796
TI **Flash memory** integrated circuit has selector circuitry which connects output terminal of address register to selected target according to control input logic.
DC U13 U14
IN CHEN, H S; HUNG, C H; LIAO, K Y; WAN, R L
PA (MACR-N) **MACRONIX INT CO LTD**
CYC 1
PI US 6178132 B1 20010123 (200157)* 9p G11C008-00 <--
ADT US 6178132 B1 US 1999-391917 19990909
PRAI US 1999-391917 19990909
IC ICM G11C008-00
AB US 6178132 B UPAB: 20011005
NOVELTY - The secondary circuits of a selector circuitry are connected to the respective output terminals of an address register (31) and address decoders (13,22). The selector circuitry connects the output terminal of the address register to a target, selected from targets including the address decoders, according to a control input logic (40).

DETAILED DESCRIPTION - The primary circuits of a selector circuitry are connected to the respective address input terminals of an address register (31) and address decoders (13,22). An INDEPENDENT CLAIM is also included for a first **floating gate** memory cell array reading method.

USE - Flash memory integrated circuit.

ADVANTAGE - Provides integrated circuit with read while write capability that is simple, consumes less IC area, and can be cost effectively manufactured.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic block diagram of flash memory IC.

Address decoders 13,22
Address register 31
Control input logic 40

Dwg.1/4
FS EPI
FA AB; GI
MC EPI: U13-C04B2; U13-E03; U14-A03B7; U14-A07; U14-A08A

L8 ANSWER 6 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:569738 HCAPLUS
DN 135:130905
TI Method for manufacturing **flash memory** device with dual **floating gates** and two bits per cell
IN Huang, Chong-jen; Chen, Hsin-huei; Liu, Lenvis; Wang, Tony; Chiou, Frank
PA **Macronix International Co., Ltd., Taiwan**
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-8247
NCL 438264000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6271090	B1	20010807	US 2000-742225	20001222 <--

AB A method for manufg. a flash memory device with dual **floating gates** is disclosed. The method use a self-aligned etching technique to form dual **floating gates** by using dual spacers as masks. First of all, a semiconductor substrate having a 1st insulating layer thereon and a 1st conductive layer formed over the 1st insulating layer is provided. Then a 2nd insulating layer is formed and patterned to etch to form a trench therein. Next a dielec. layer is deposited and anisotropically etched to form dual spacers in the trench. After removing the 2nd insulating layer, etching the 1st conductive layer to expose the 1st insulating layer, and removing the spacers sequentially, dual **floating gates** are formed. Two doped regions sep. located on 2 sides of the dual **floating gates** are then formed by using photolithog. and an ion implantation process. After thickening the 1st insulating layer, a composite layer, a 2nd conductive layer and a 3rd insulating layer is formed over the semiconductor substrate sequentially.
ST semiconductor device fabrication flash memory dual **floating gate**
IT Etching
(anisotropic; method for manufg. flash memory device with dual **floating gates** and two bits per cell)
IT Films
(elec. conductive; method for manufg. flash memory device with dual **floating gates** and two bits per cell)
IT Electric conductors
(films; method for manufg. flash memory device with dual **floating gates** and two bits per cell)
IT Semiconductor memory devices
(flash; method for manufg. flash memory device with dual **floating gates** and two bits per cell)
IT Dielectric films
Doping
Electric insulators
Ion implantation
Photolithography
Photomasks (lithographic masks)
Semiconductor device fabrication
(method for manufg. flash memory device with dual **floating gates** and two bits per cell)
IT 7440-21-3, Silicon, uses 7631-86-9, Silica, uses 12033-89-5, Silicon nitride, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(method for manufg. flash memory device with dual **floating**

gates and two bits per cell)
RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
RE
(1) Hara; US 5492846 1996
(2) Hsu; US 6197637 2001 HCAPLUS
(3) Liang; US 5714412 1998 HCAPLUS
(4) Mitchell; US 5143860 1992
(5) Sheu; US 5646059 1997 HCAPLUS

L8 ANSWER 8 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:640648 HCAPLUS
DN 131:251361
TI **Floating gate flash memory** with substrate band-to-band tunneling induced hot electron injection for allowing programming operations significantly faster than prior approaches
IN Guo, Jyh-Chyurn; Tsai, W. J.
PA **Macronix International Co., Ltd., Taiwan**
SO Eur. Pat. Appl., 30 pp.
CODEN: EPXXDW
DT Patent
LA English
IC ICM H01L029-788
ICS G11C016-04
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 948058	A1	19991006	EP 1998-302631	19980403
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	US 6352886	B2	20020305	US 2001-753788	20010103 <--
PRAI	US 1998-41807	A	19980313		
	US 1999-473849	B3	19991228		

AB A new flash memory cell structure and operational bias approach for allowing programming operations significantly faster than prior approaches, is based on the use of band-to-band tunneling induced hot electron injection in cells to be programmed, and in one embodiment on the use of triple-well **floating gate** memory structures. The method of preferred embodiments comprises inducing band-to-band tunneling current from the semiconductor body to one of the source and drain near the channel, and applying a pos. bias voltage to the control gate to induce hot electron injection into the **floating gate**. The other of the source and drain terminals is floated, that is disconnected so that current does not flow through that terminal. The band-to-band tunneling current is induced by applying a ref. potential to one of the source and drain sufficient to establish conditions for the band-to-band tunneling current. For example, a ref. potential of .apprx.0 V is applied to the drain, and neg. bias of .apprx.-4 V to -8 V is applied to the semiconductor body, and a pos. voltage is applied to the control gate which falls in a range of .apprx.+6 V to .apprx.+10 V.

ST programming flash **floating gate** memory; fabrication flash **floating gate** memory
IT Semiconductor materials
(doped; **floating gate** flash memory with substrate band-to-band tunneling induced hot electron injection for allowing programming operations significantly faster than prior approaches)
IT Semiconductor memory devices
(flash; **floating gate** flash memory with substrate band-to-band tunneling induced hot electron injection for allowing programming operations significantly faster than prior approaches)
IT Doping
Ion implantation
Semiconductor device fabrication
(**floating gate** flash memory with substrate band-to-band tunneling induced hot electron injection for allowing programming operations significantly faster than prior approaches)
RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
RE
(1) Chen; US 5739569 A 1998 HCAPLUS
(2) Chen, I; PROCEEDINGS OF THE INTERNATIONAL ELECTRON DEVICES MEETING, WASHINGTON, DEC 3 - 6, 1989 1989, P263

(3) Fujitsu Ltd; JP 05226665 A 1993
(4) Kawasaki Steel Corp; JP 05315625 A 1993
(5) Mitsubishi, D; DE 19600544 A 1996
(6) Texas Instruments Incorporated; EP 0399261 A 1990

L8 ANSWER 7 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:449233 HCAPLUS
DN 135:27968
TI Method for forming a V-shaped **floating gate** with reduced lateral dimensions for **flash memory** cells
IN Huang, Chin-yi; Chang, Yun; Pan, Samuel C.
PA **Macronix International Co., Ltd., Taiwan**
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-8242
ICS H01L021-336
NCL 438260000
CC 76-3 (Electric Phenomena)
FAN.CNT 4

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6248631	B1	20010619	US 1999-415788	19991008 <--
	US 2001042882	A1	20011122	US 2001-818078	20010327 <--
PRAI	US 1999-415788	A2	19991008		
	US 1999-415936	A2	19991008		
	US 1999-415938	A2	19991008		
	US 1999-415939	A2	19991008		

AB The invention provides a **floating gate** memory cell, where the **floating gate** comprises a 1st lateral end region and a 2nd lateral end region. A middle region is positioned towards a middle of the **floating gate** with respect to the 1st lateral end region and the 2nd lateral end region. The thickness of the **floating gate** decreases continuously from at least one of the 1st or 2nd lateral end regions to the middle region. This invention also provides for a method of forming a contoured **floating gate** for use in a **floating gate** memory cell. The method includes forming a polysilicon structure between a 1st alignment structure and a 2nd alignment structure, where the polysilicon structure has a max. thickness at a 1st lateral end region adjacent to the 1st alignment structure and at a 2nd lateral end region adjacent to the 2nd alignment structure, and where the polysilicon structure has a min. thickness at a middle region positioned between the 1st lateral end regions and the 2nd lateral end region. The method further includes forming a polysilicon layer over the polysilicon structure such that the polysilicon layer adopts a contour of the polysilicon structure.

ST V shaped **floating gate** flash memory fabrication
IT Memory devices
(EPROM (erasable programmable read-only); method for forming V-shaped **floating gate** with reduced lateral dimensions for flash memory cells)
IT Gate contacts
Nonvolatile memory devices
Semiconductor memory devices
(method for forming V-shaped **floating gate** with reduced lateral dimensions for flash memory cells)
IT 7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(poly; in method for forming V-shaped **floating gate** with reduced lateral dimensions for flash memory cells)
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
RE
(1) Kitamura; 1998 Symposium on VLSI Technology
(2) Liang; US 5923974 1999 HCAPLUS

(3) Miles; US 6069040 2000 HCAPLUS
(4) Tseng; US 5677216 1997 HCAPLUS